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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HERB H. HUANG,
HAITING LI, and WEN XU

Appeal 2009-004378
Application 10/773,522
Technology Center 2800

Decided: September 23, 2009

Before KENNETH W. HAIRSTON, JOHN C. MARTIN,
and ROBERT E. NAPPI, *Administrative Patent Judges*.

HAIRSTON, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134 from the Examiner's final rejection of claims 1 to 10.[1] We have jurisdiction under 35 U.S.C. § 6(b).

We will sustain the rejections.

Appellants' invention is concerned with a method for manufacturing ROM memory devices (Spec. ¶ [04]), and an improved method for doing so by forming an isolation trench structure and a refractory metal layer (Abstract).

Claim 1, reproduced below, is representative of the subject matter on appeal:

1. A method for manufacturing ROM memory devices, the method comprising:

forming a trench isolation structure within a cell region of a semiconductor substrate, the cell region being in an array region for ROM memory devices, the trench isolation structure being provided to separate a continuous bit line region of the cell from another continuous bit line region from another cell;

forming a gate structure within the cell region;

forming a first sidewall spacer overlying a first side of the gate structure and a second sidewall spacer overlying a second side of the gate structure, each of the sidewall spacers including the first sidewall spacer and the second sidewall spacer being configured to extend over and overlap a portion of the trench isolation structure and to extend over and overlap a portion of source/drain regions, each of the sidewall spacers including the first sidewall spacer and the second sidewall spacer being adapted to separate the gate structure from the trench isolation region and to separate the gate structure from the source/drain regions;

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[1] Claims 11 to 26 have been canceled.

applying a refractory metal layer overlying the gate structure including the first side wall spacer and the second sidewall spacer and exposed portion of the trench isolation structure;

alloying the refractory metal layer to the gate structure and exposed portions of source/drain regions to form silicided regions overlying the gate structure and source/drain regions; and

selectively removing the refractory metal layer from the sidewall spacers and exposed portion of the trench isolation structure.

The Examiner relies upon the following as evidence of unpatentability:

Chang	US 5,506,160	Apr. 9, 1996
Shiau	US 6,372,580 B1	Apr. 16, 2002
Iwata	US 2004/0262650 A1	Dec. 30, 2004
Yang	US 6,847,087 B2	Jan. 25, 2005

The following rejections are before us for review:

Claims 1 to 4 and 6 to 8 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Shiau and Yang.

Claims 5 and 9 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Shiau and Yang, further in view of Iwata.

Claim 10 stands rejected under 35 U.S.C. § 103(a) as unpatentable over Shiau and Yang, further in view of Chang.

The Examiner relies upon Shiau as describing all of the features of a method for manufacturing ROM memory devices having a gate structure, first and second sidewall spacers, and a refractory metal layer, as set forth in claim 1 (Ans. 3-4). The Examiner relies upon Yang as describing a trench isolation structure (Ans. 4-5).

Appellants argue (App. Br. 6-8; Reply Br. 1-3), *inter alia*, that (i) there is no suggestion in Shiau to combine it with Yang (App. Br. 6), (ii) Shiau and Yang have conflicting functions and inconsistent objectives since Shiau's silicide (i.e., refractory metal) layer is for reducing electrical resistance in word and bit lines while Yang's contact plug is for short-circuiting drain and bit lines, and that as a result (iii) the Examiner employed hindsight in making the combination. Appellants also argue (Reply Br. 2-3) that Shiau fails to teach forming a trench isolation structure and Yang fails to teach forming a silicide.

Appellants make the foregoing arguments based on an analysis of claim 1 with respect to the teachings of Shiau and Yang.[2] Independent claim 1 is representative of the group of claims consisting of claims 1 to 4 and 6 to 8 which stand rejected under 35 U.S.C. § 103(a) as unpatentable over Shiau and Yang. *See* 37 C.F.R. § 41.37(c)(1)(vii).

ISSUE

Based on Appellants' arguments, the issue is: Have Appellants demonstrated that the Examiner erred in concluding that it would have been obvious to one of ordinary skill in the art to combine the method of making ROM memory devices having refractory metal layers taught by Shiau with the step of forming a trench isolation structure taught by Yang?

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[2] *See* App. Br. 6-8; Reply Br. 2-3 (Appellants present specific arguments only as to claim 1). *See also* App. Br. 8 (Appellants present nominal arguments as to remaining claims 2 to 10, relying on the substance of the arguments with regard to claim 1 for patentability of the remaining claims).

FINDINGS OF FACT

1. As indicated *supra*, Appellants describe and claim a method for manufacturing ROM memory devices having buried bit lines (Figs. 1, 3-5; Abstract; Spec. ¶¶ [10], [11]; Title). Each ROM memory device includes a trench isolation structure 101 which separates continuous bit lines 105 from each other, a gate structure including gate dielectric layer 309, first and second sidewall spacers 201, and a refractory metal layer 305 and 307 (*see* Figs. 3-5). Trench isolation structure 101 has a depth greater than the bit lines 105 (Fig. 5; Spec. ¶ [24]). Appellants recognize the need for ROM memory device manufacturing methods to have improved interconnect and isolation structures (Spec. ¶ [04]).
2. Shiau describes a method for manufacturing ROM memory devices having continuous buried bit lines (*see generally* Fig. 4; Abstract; col. 4, l. 48 to col. 5, l. 21). Shiau describes applying, heat treating (i.e., alloying), and selectively etching (i.e., removing) a refractory metal layer (e.g., titanium) (Figs. 11A-11D; col. 4, l. 56 to col. 5, l. 4).
3. Yang, like both Shiau and Appellants, describes a method for manufacturing ROM memory devices having continuous buried bit lines (Figs. 2(a)-(c); Abstract). Yang isolates buried bit lines (SPW) from each other with shallow trench isolation (STI) regions. The STI layer has a depth which is greater than the depth of the isolated bit lines (col. 4, ll. 48-50).

4. Yang, like Appellants, discloses providing an isolation trench thickness greater than the depth of the buried bit lines to isolate the bit lines from each other (col. 4, ll. 44-47).

PRINCIPLES OF LAW

The test for obviousness is what the combined teachings of the references would have suggested to the artisan. Accordingly, one can not show nonobviousness by attacking references individually where the rejection is based on a combination of references. *In re Keller*, 642 F.2d 413, 426 (CCPA 1981).

It is necessary to consider "common sense-in … deciding in which fields a person of ordinary skill would reasonably be expected to look for a solution to the problem facing the inventor." *In re Oetiker*, 977 F.2d 1443, 1447 (Fed. Cir. 1992).

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. *See In re Fine*, 837 F.2d 1071, 1073 (Fed. Cir. 1988). The Examiner's articulated reasoning in the rejection must possess a rational underpinning to support the legal conclusion of obviousness. *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006).

The Examiner bears the initial burden of presenting a prima facie case of obviousness, and Appellants have the burden of presenting a rebuttal to the prima facie case. *Oetiker*, 977 F.2d at 1445. Appellants have the burden on appeal to the Board to demonstrate error in the Examiner's position. *See Kahn*, 441 F.3d at 985-86.

ANALYSIS

Claims 1 to 4 and 6 to 8

We will sustain the Examiner's rejection with respect to representative claim 1 for the reasons that follow. We agree with the Examiner's findings of fact and conclusions of obviousness with respect to claim 1 (Ans. 3-6), and adopt them as our own, along with some amplification of the Examiner's explanation of the teachings of Shiau (FF 2) and Yang (*see* FF 3, 4). *See Fine*, 837 F.2d at 1073; *Kahn*, 441 F.3d at 988.

Representative claim 1, as well as claims 2 to 10 which ultimately depend on claim 1, all recite a method including "forming a trench isolation structure" and forming (i.e., applying, alloying and selectively removing) a "refractory metal layer" (claim 1).

As indicated *supra* (FF 2), Shiau describes the salient features of claim 1 including forming a refractory metal layer. Yang describes forming an isolation trench structure for the purpose of isolating buried bit lines (FF 3, 4). We agree with the Examiner that both Shiau and Yang are from the same field of endeavor (Ans. 5), manufacturing ROM devices with buried bit lines (*see* FF 2, 3). We also agree with the Examiner that it would have been obvious to modify Shiau with the isolation trench structure teaching of Yang in order to provide isolation for the bit lines of Shiau (Ans. 5).

The Examiner has provided articulated reasoning with a rational underpinning to support the combination for the legal conclusion of obviousness (Ans. 3-5). *See Kahn*, 441 F.3d at 988. Appellants have failed to rebut the Examiner's showing that Shiau and Yang teach or suggest all of the limitations of claim 1. Appellants notably admit (Reply Br. 2) that Yang

"does show trench isolation" in Fig. 2(a). In view of our discussion as to the teachings and suggestions of Shiau and Yang *supra*, Appellants have not demonstrated that the Examiner erred in relying on the combination of Shiau and Yang as teaching or suggesting a method of manufacturing ROM devices including forming an isolation trench layer and a refractory metal layer, as set forth in claim 1.

Appellants' arguments (App. Br. 6) that the Examiner erred in combining Shiau with Yang due to a lack of motivation being found in Shiau is unpersuasive since both Shiau and Yang teach or suggest methods of making ROM memory devices having buried bit lines (FF 2, 3), and since the motivation, to provide isolation of bit lines, is disclosed by Yang (FF 3). In fact, Yang achieves isolation, in a similar fashion as Appellants, by forming an isolation trench between bit lines that has a greater depth than the bit lines to be isolated (*compare* FF 1 *with* FF 4).

With regard to Appellants' arguments (App. Br. 7; Reply Br. 3) that the silicide (i.e., refractory metal) layer of Shiau and the contact plug of Yang have conflicting and inconsistent functions, this argument is unpersuasive in light of the Examiner's reliance on Yang only for forming a trench isolation structure. The Examiner has not relied upon Yang for teaching a contact plug (*see* Ans. 4-5, 8-9), instead "[t]he Yang patent was relied upon solely for the teaching of a trench isolation structure between adjacent buried bit lines" (Ans. 8).

Appellants' contentions that the Examiner employed impermissible hindsight in combining Shiau with Yang (App. Br. 6-8; Reply Br. 2-3) are unpersuasive since both Shiau and Yang are in the analogous art of

semiconductor ROM devices having buried bit lines, and for the reasons that follow. *Cf. Oetiker*, 977 F.2d at 1447 (stating that the hindsight combination of non-analogous sources to reconstruct applicants' invention "is insufficient to present a *prima facie* case of obviousness"); *also cf.* FF 1 discussing Appellants' invention *and* FF 2 relating to the teachings of Shiau *with* FF 3 relating to the teachings of Yang.

Only "common sense" would have been necessary for a person of ordinary skill to look to Yang for a solution to the problem of providing an improved memory device, especially one capable of isolating bit lines. *See Oetiker*, 977 F.2d at 1447. Common sense would have led one of ordinary skill in the art of making ROM devices having buried bit lines to look to the ROM device having trench isolation structures of Yang (*see* FF 3, 4) to solve the problem of isolating bit lines. Appellants, like Yang, recognize that such a problem can be solved by forming trench isolation structures having a depth greater than the depth of the bit lines they are to isolate (*cf.* FF 1 *with* 4).

Appellants argue that (i) Shiau provides no suggestion to motivate the ordinarily skilled artisan to combine Shiau with Yang (App. Br. 6), (ii) Shiau fails to teach formation of a trench isolation structure (Reply Br. 2), and (iii) Yang fails to teach forming a silicide (i.e., refractory metal layer) (Reply Br. 2). These arguments are unpersuasive. The test for obviousness is what the *combined* teachings of the references would have suggested to the artisan. Accordingly, one can not show nonobviousness by attacking references individually where the rejection is based on a combination of references. *Keller*, 642 F.2d at 426. In the instant case, Appellants' argument are not

persuasive since the Examiner relied upon *Yang* as teaching the limitation of forming a trench isolation structure, and *Shiau* as teaching the limitation of forming a refractory metal layer (*see* Ans. 4-5; FF 2, 3). The Examiner is correct that (i) Yang teaches forming a trench isolation structure for the purpose of isolating buried bit lines (Ans. 4-5, 8; FF 3, 4), and (ii) therefore the motivation for combining the teachings of Shiau and Yang need not come from Shiau (Ans. 7-8). In view of the foregoing, Appellants have not demonstrated that the Examiner used impermissible hindsight in combining Shiau and Yang, or that the obviousness rejection is otherwise in error.

In view of the foregoing, we will sustain the obviousness rejection of claim 1 based upon the teachings of Shiau and Yang. The same holds true for claims 2 to 4 and 6 to 8, which depend from claim 1, because Appellants have not presented any patentability arguments for these claims apart from the arguments presented for claim 1 (*see* App. Br. 8).

Claims 5, 9, and 10

We agree with the Examiner's findings of fact and conclusions of obviousness with respect to claims 5, 9, and 10 (Ans. 6-7), and adopt them as our own. The Examiner has provided articulated reasoning with a rational underpinning to support a legal conclusion of obviousness based upon the teachings of the applied references (Ans. 3-7). Once the Examiner has satisfied the burden of presenting a prima facie case of obviousness, the burden then shifts to Appellants to present evidence and/or arguments that persuasively rebut the Examiner's prima facie case. *See Oetiker*, 977 F.2d at 1445.

Appellants have not presented any patentability arguments as to claims 5, 9, and 10, other than asserting that Iwata and Chang do not appear to cure the deficiencies of Shiau and Yang (*see* App. Br. 8). Appellants' arguments do not show error in the Examiner's prima facie case of obviousness put forth in the Examiner's Answer (*see* Ans. 3-7), and are unconvincing in light of our findings and conclusions with respect to the obviousness rejection based on the teachings of Shiau and Yang.

Since Appellants have not particularly pointed out errors in the Examiner's reasoning to persuasively rebut the Examiner's prima facie case of obviousness, the § 103 rejections of (i) claims 5 and 9 based on Shiau, Yang, and Iwata, and (ii) claim 10 based on Shiau, Yang, and Chang are therefore sustained.

CONCLUSION OF LAW

Appellants have not shown that the Examiner erred in concluding that it would have been obvious to one of ordinary skill in the art to combine the method of making ROM memory devices including refractory metal layers taught by Shiau, with the step of forming a trench isolation structure taught by Yang.

ORDER

The decision of the Examiner to reject claims 1 to 10 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

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